LZ95G65

Single-chip Driver LSI for CCD

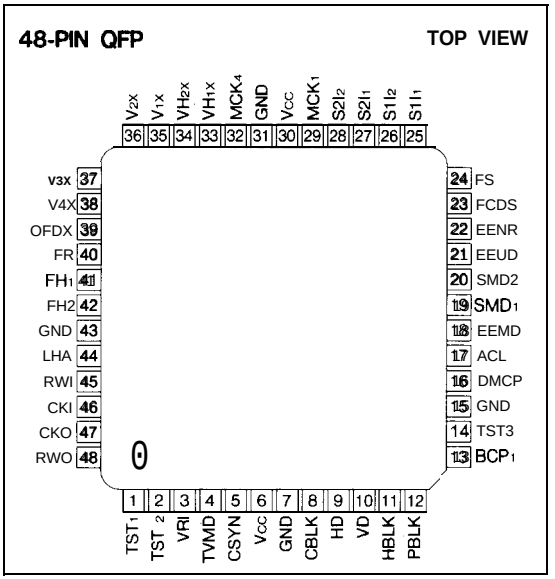
DESCRIPTION

The LZ95G65 is a CMOS single chip driver LSI which provides timing pulses used to drive a CCD area sensor, and generates synchronous pulses for TV signals and processing pulses for video signals,

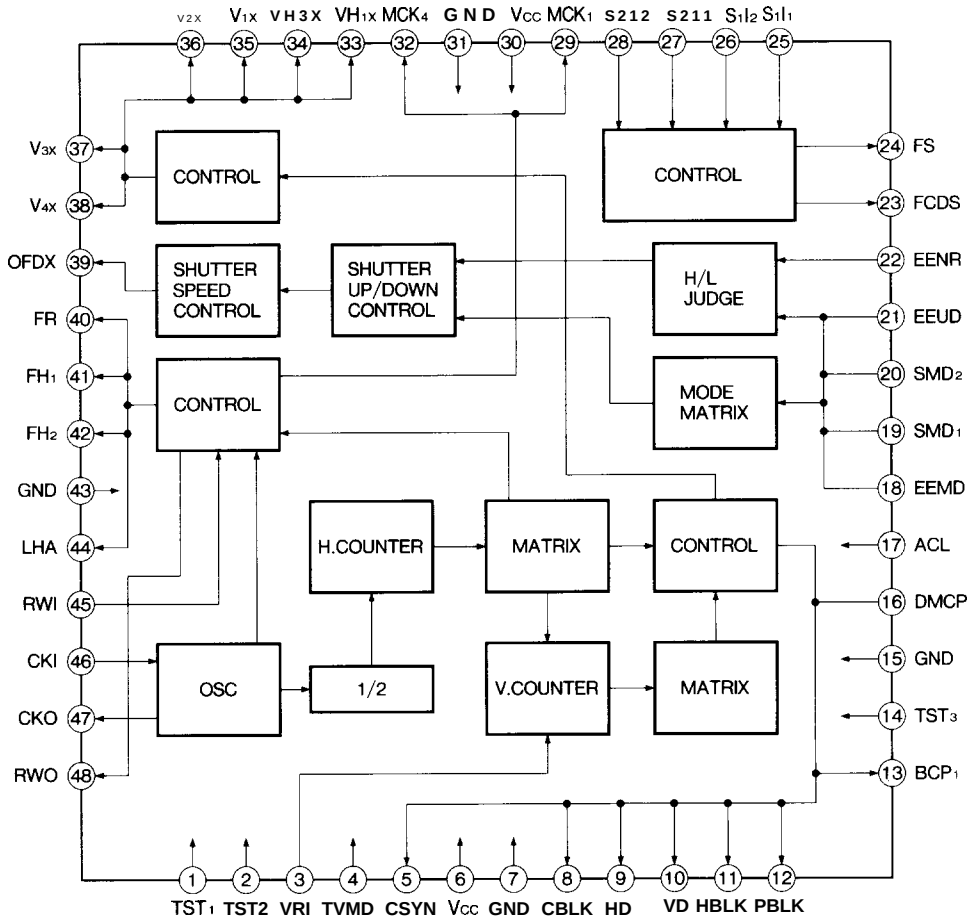
FEATURES

- Switchable **between 410000 pixels B/W CCD and 470000 pixels B/W CCD**
- Switchable **between EIA and CCIR systems**
- **Built-in EE (Electronic Exposure) control (1/60 to 1 /50 000 s for EIA; 1 /50 to 1 /50 000 s for CCIR)**
- **Internal electronic shutter :**
  Shutter speed is selectable from 1/~ (EIA : 1 /50), 1/1 25, 1 /250, 1 /500, 1/1 000, 1/2 000, 1/4 000 and 1/1 O 000 s, in addition to this, 1/1 00 s in flicker-less mode using parallel code
- Switchable **between Electronic Shutter mode and EE Control mode**
- **External vertical synchronization is possi ble**
- **Single +5 V power supply**
- **Package : 48-pin QFP(QFP048-P-101 O)**

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power voltage	V_{CC}	– 0.3 to 7.0	v
Input voltage	V_I	– 0.3 to V_{CC} + 0.3	v
Output voltage	V_O	– 0.3 to V_{CC} + 0.3	v
Operating temperature	Topr	–30 to +75	℃
Storage temperature	Tstg	–55 to +150	"c

DC CHARACTERISTICS

(V_{CC} = +5.0 V ± 10%, Ta = −30 to +75℃)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Low level input voltage	V_{IL}				1.5	v	1
High level input voltage	V_{IH}		3.5			v	
Low level input current	$\lvert I_{IL1} \rvert$	V_I = 0 V			1.0	μA	2
	$\lvert I_{IL2} \rvert$	V_I = 0 V	6.0		75	μA	3
High level input current	$\lvert I_{IH1} \rvert$	V_I = V_{CC}			1.0	μA	4
	$\lvert I_{IH2} \rvert$	V_I = V_{CC}	6.0		75	μA	5
High level output voltage	$V_{OH}1$	I_{OH} = −1.6 mA	4.0			v	6
Low level output voltage	V_{OL1}	I_{OL} = 3.2 mA			0.4	v	
High level output voltage	V_{OH2}	I_{OH} = −4.8 mA	4.0			v	7
Low level output voltage	V_{OL2}	I_{OL} = 9.6 mA			0.4	v	
High level output voltage	V_{OH3}	I_{OH} = – 7.2 mA	4.0			v	8
Low level output voltage	V_{OL3}	I_{OL} = 14.4 mA			0.4	v	
High level output voltage	V_{OH4}	I_{OH} = – 9.6 mA	4.0			v	9
Low level output voltage	V_{OL4}	I_{OL} = 19.2 mA			0.4	v	

NOTES :

1. Applied to inputs (IC, ICD, ICU, IBF0)
2. **Applied to inputs** (IC, ICD, IBF0).
3. **Applied to input** (ICU).
4. **Applied to inputs** (IC, **ICU,** IBF0).
5. **Applied to input (ICD).**
6. **Applied to outputs (O, ORI,** OSC).
7. **Applied to output** (O6R22).
8. **Applied to output (06** R23).
9. **Applied to output (06** R24).

PIN FUNCTION

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
1	TSTI	ICD	–	Test terminal 1	Testing pin. Typically connected to the GND level.
2	TST2	ICD	–	Test terminal 2	Testing pin. Typically connected to the GND level.
3	VRI	ICU	⎍	Vertical reset input	An input pin for resetting internal vertical counter. The falling edge of input pulse is necessary within 1/2 horizontal period from vertical synchronous start point. Set to H level when not resetting.
4	TVMD	ICU	–	TV mode select	An input pin to select TV standards. At EIA mode : H level At CCIR mode : L level
5	CSYN	OR1	⎍	Composite synchronizing pulse	A composite synchronous signal
6	Vcc	–	–	Power supply	Supply +5 V power.
7	GND	–	–	Ground	A grounding pin.
8	CBLK	OR1	⊓	Composit blanking pulse	Composite blanking pulses.
9	HD	OR1	⎍	Horizontal drive pulse	The pulse occurs at the start of lines.
10	VD	OR1	⎍	Vertical drive pulse	The pulse occurs at the start of every field.
11	HBLK	OR I	⎍	Horizontal blanking pulse	A pulse that corresponded to the rest period of the horizontal transfer pulse.
12	PBLK	ORI	⎍	Pre-blanking pulse	Equivalent to CBLK (pin 8) pulse except for shorter pulse width with cutt-off falling edge.
13	BCP_1	ORI	⎍	Optical black clamp pulse	A pulse to clamp the optical black signal.
14	TST3	ICD	–	Terminal 3	Testing pin. Typically connected to the GND level.
15	GND	–	–	Ground	A grounding pin.
16	DMCP	OR1	-	Dummy clamp pulse	A pulse to clamp the dummy signal.
17	ACL	ICU	⎍	All clear input	An input pin to reset at power on For details, sea “NOTE 1”.
18	EEMD	ICU	–	Electronic Exposure mode select	An input pin to select electronic shutter function. At Fixad mode : L level At EE mode : H level
19	SMD_1	ICU	–	Shutter control 1	Input pins to set up Fixed Shutter Speed or to control Electronic Exposure mode. For details, see “NOTE 2, 3“.
20	SMD2	ICU	–	Shutter control 2	
21	EEUD	ICU	–	Electronic Exposure control 1	
22	EENR	ICU	-	Electronic Exposure control 2	
23	FCDS	O6R22	⎍	CDS pulse 1	A pulse to clamp CCD output signals.

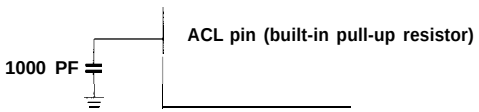
PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
24	FS	06R22	⎍	CDS pulse 2	A pulse to sampling CCD output signals.
25	S1I1	IC	–	Phase of FCDS control input 1	An input pin to control the phase of FCDS (pin 23). To be connected to the MCK4 (pin 32).
26	S1I2	IC	–	Phase of FCDS control input 2	An input pin to control the phase of FCDS (pin 23). To be connected to the MCK 1 (pin 29).
27	S2I1	IC	–	Phase of FS control input 1	An input pin to control the phase of FS (pin 24). To be connected to the MCK4 (pin 32).
28	S212	IC	–	Phase of FS control input 2	An input pin to control the phase of FS (pin 24). To be connected to the MCK 1 (Pin 29).
29	MCK 1	o	–	Clink output 1	Pin to output 1/2 frequency of CKI (pin 46). To be connected to the S1 I2 (pin 26) and S212 (pin 28).
30	Vcc	–	–	Power supply	Supply +5 V power.
31	GND	–	–	Ground	A grounding pin.
32	MCK4	o	–	Clock output 4	Pin to output 1/2 frequency of CKI (pin 46). To be connected to the S1 I1 (pin 25) and S211 (pin 27).
33	VHIX	ORI	⎾⎍	Read out pulse 1	An output pin to transfer the photodiode charge of CCD to the vertical shift register. To be connected to the 1 BX pin of the LR36683N vertical driver LSI.
34	VH2X	OR1	⎾⎍	Read out pulse 2	An output pin to transfer the photodiode charge of CCD to the vertical shift register. To be connected to the 3BX pin of the LR36683N vertical driver LSI.
35	VI X	ORI	⎍	Vertical transfer pulse 1	Vertical transfer pulse. To be connected to the 1 AX pin of the LR36663N vertical driver LSI.
36	V2X	OR I	n	Vertical transfer pulse 2	Vertical transfer pulse. To be connected to the 2AX pin of the LR36663N vertical driver LSI.
37	V3X	OR1	⎾⎍	Vertical transfer pulse 3	Vertical transfer pulse. To be connected to the 3AX pin of the LR36663N vertical driver LSI.
38	V4X	OR I	V	Vertical transfer pulse 4	Vertical transfer pulse. To be connected to the 4AX pin of the LR36663N vertical driver LSI.
39	OFDX	o	⎾⎍	OFD pulse output	An output pin to sweep the photodiode charge of CCD. When EEMD = SMD2 = SMD1 = L, a pulse becomes H level signal.
40	FR	06R23	⎍	Reset pulse	A reset pulse for CCD. Connect to ϕ_R of CCD through the DC offset circuit.
41	FH 1	06R24	⎍	Horizontal transfer pulse 1	Horizontal transfer pulse.

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
42	FH2	06R24	⌐	Horizontal transfer pulse 2	Horizontal transfer pulse.
43	GND	–	–	Ground	A grounding pin.
44	LHA	06R22	⌐	Horizontal transfer last pulse	A pulse to drive the last gate of horizontal CCD.
45	RWI	IC	⌐	Width of FR control input	An input pin to control the phase of FR (pin 40)
46	CKI	IBF0	⌐⌐	Clink input	A pin for oscillation inverter input. EIA : 1820 fH, CCIR : 1816 fH (fH=Horizontal frequency)
47	CKO	Osc	⌐⌐	Clock output	A pin for oscillation inverter output.
48	RWO	OR1	⌐	Width of FR control output	Pin to output 1/2 frequency of CKI (pin 46). To be connected to the RWI (pin 45).

IC : Input pin (CMOS level).
ICU Input pin (CMOS level with built-in pull-up resistor).
ICD Input pin (CMOS level with built-in pull-down resistor)
IBF0 Input pin for oscillation.
Osc Output pin for oscillation.
0 Output pin.
OR1 Output pin.
06R22 Output pin.
08R23 Output pin.
06R24 Output pin.

NOTES :

1. How to use ACL pin (Pin 17)

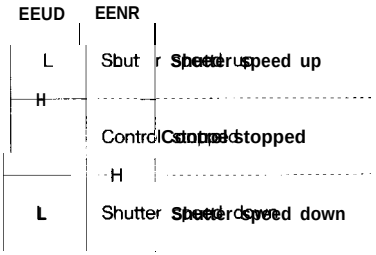


2. Fixed Shutter mode
EEMD (Pin 18) = Low level

EEUD (Pin 21)	SMD2 (Pin 20)	SMD1 (Pin 19)	SHUTTER SPEED (S)	
			EIA	CCIR
L	L	L	About 1/60	About 1/50
L	L	H	About 1/100 (Flicker-less)	
L	H	L	About 1/250	
L	H	H	About 1/500	
H	L	L	About 1/1 000	
H	L	H	About 1/2 000	
H	H	L	About 1/4000	
H	H	H	About 1/1 0000	

3. EE Control mode

EEMD (Pin 18)=High level



- When EENR and EEUD are H level, control is stopped.
- When either EENR or EEUD is L level, control is resumed.

SMD_2 (Pin 20)	SMD_1 (Pin 19)	SHUTTER SPEED (S)	
		EIA	CCIR
L	L	1/60 to 1/10 000	1/50 to 1/10000
L	H	1 /60 to 1 /20 000	1 /50 to 1 /20 000
H	L	1 /60 to 1 /30 000	1 /50 to 1 /30 000
H	H	1 /60 to 1 /50 000	1 /50 to 1 /50 000

The shutter speed changes in the table as shown below

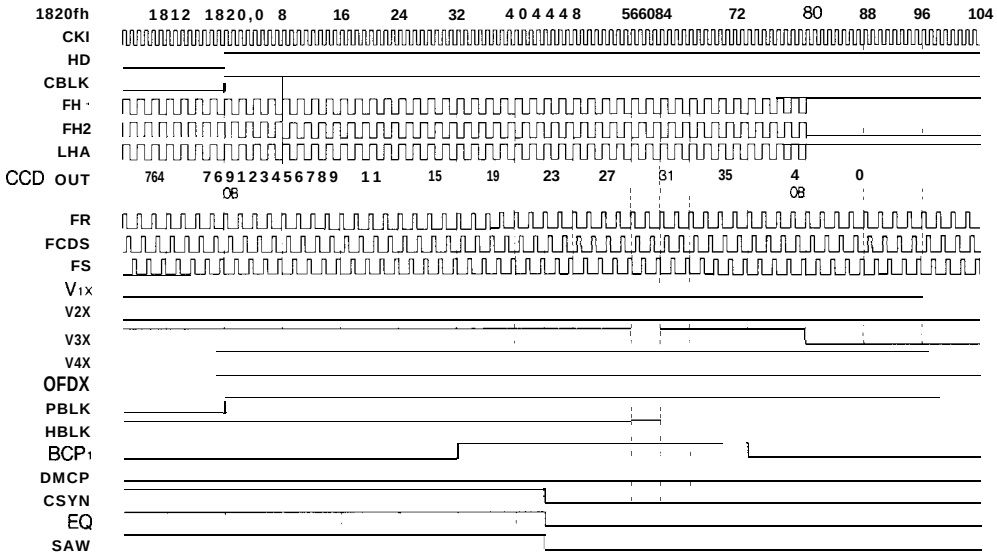
SHUTTER SPEED (S)	EIA	1/60 to 1/218	to 1 /556	to 1/1 099	to 1/2151
	CCIR	1/50 to 1/216	to 1 /552	to 1/1 091	to 1/2 136
CHANGE STEP (S)	EIA	1/1 500	1/3 900	1/7 800	1/15000
	CCIR				
SHUTTER SPEED (s)	EIA	to 1/3 647	to 1/14378	to 1 /50 083	
	CCIR	to 1/3 621	to 1/14 273	to 1 /49 606	
CHANGE STEP (S)	EIA	1 /26 000	1/47 000	1/140 000	
	CCIR	1 /35 000	1/71 000		

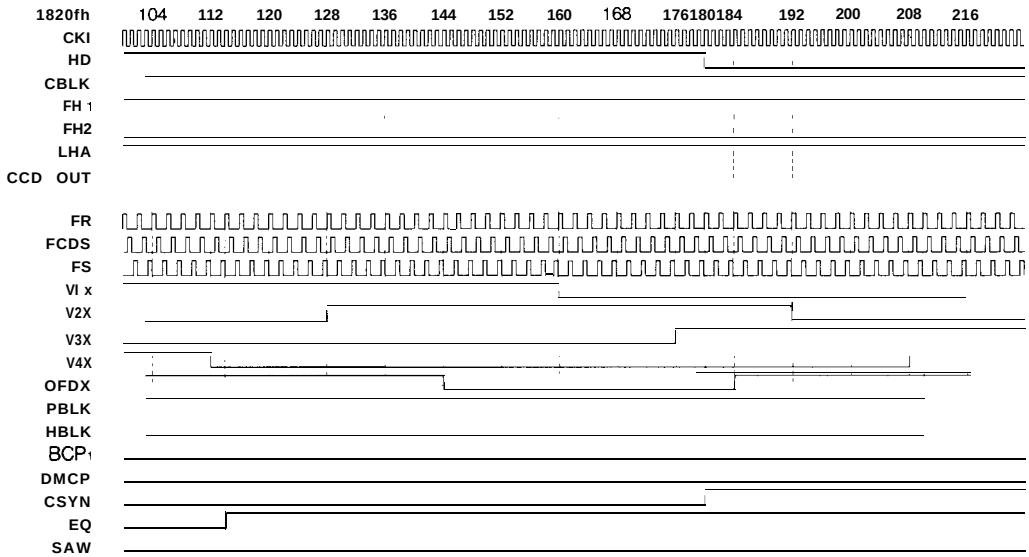
4. The output phases of FR, FS and FCDS, under the standard of rise-up in FH 1, are able to be adjusted by modifying the input phase following the combination table as ahown below.

ADJUSTED OUTPUT PHASE	MODIFIED INPUT SIGNAL
FR (only fall-down)	RWI
FS	$S2I_1$, S212
FCDS	SiII, $S1I_2$

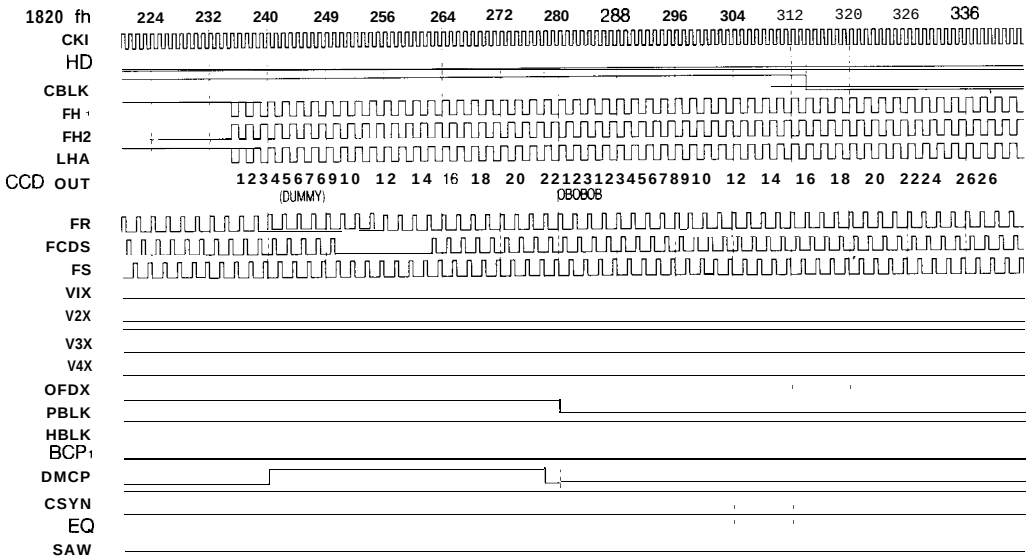
TIMING DIAGRAM

HORIZONTAL PULSE TIMING <EIA>

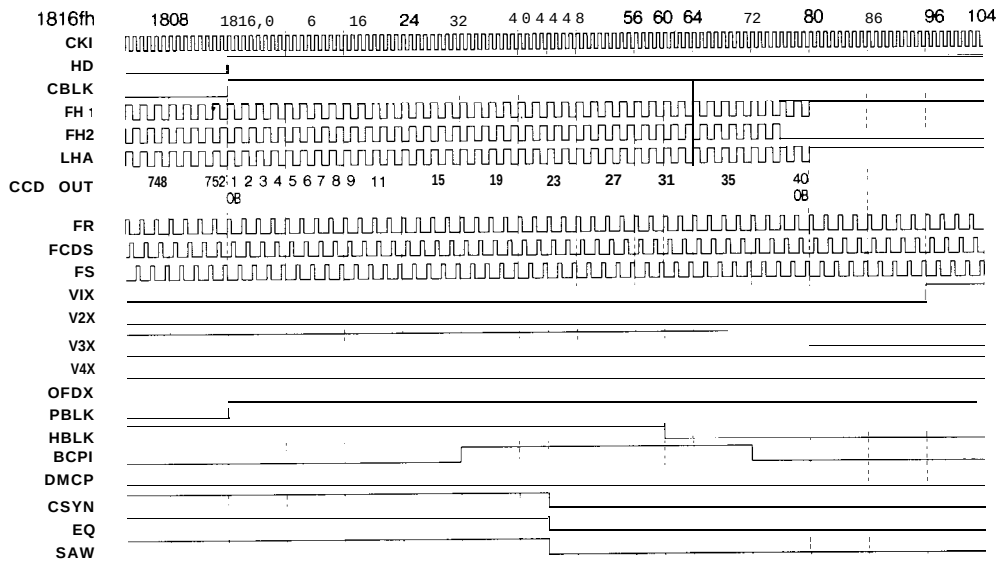




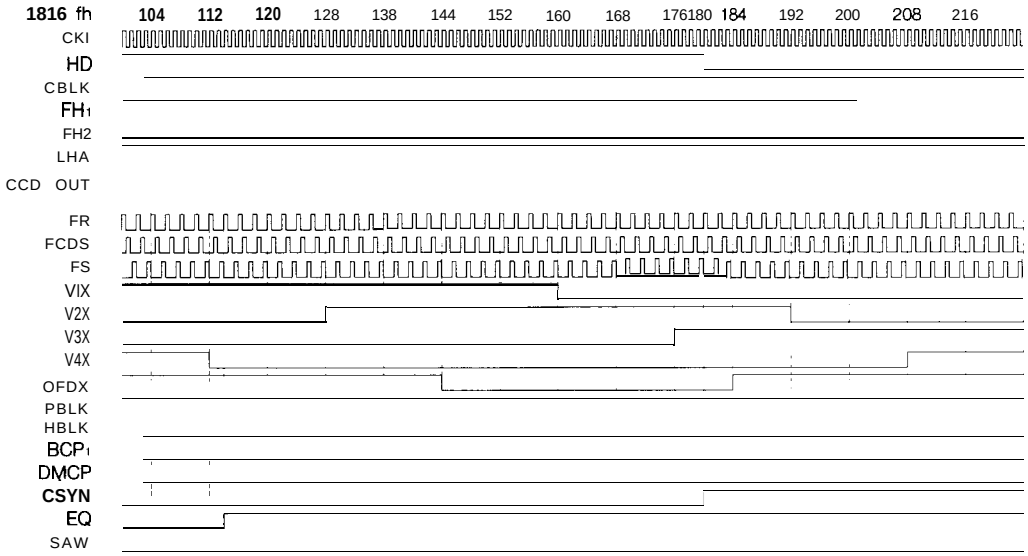
HORIZONTAL PULSE TIMING < EIA >

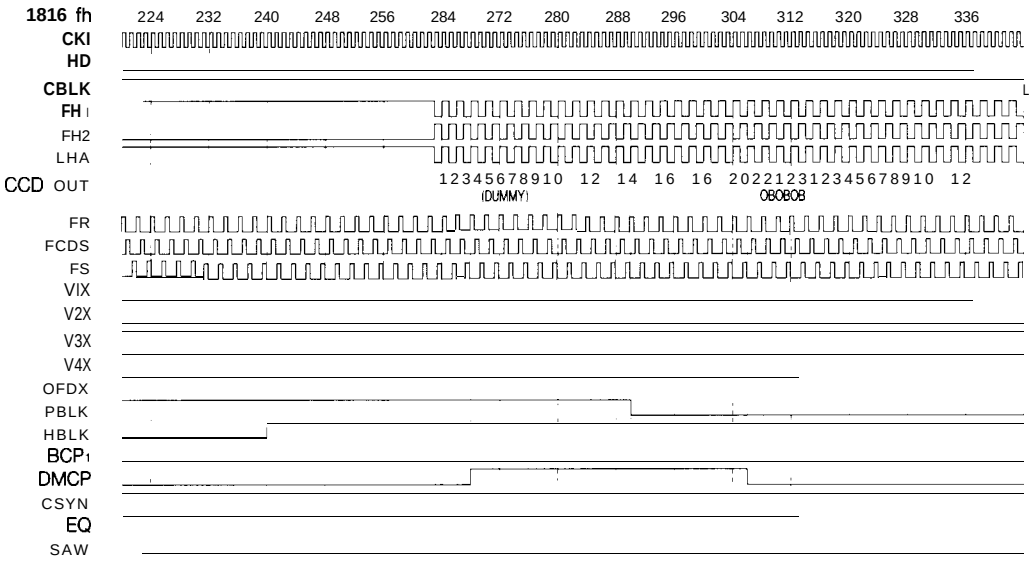


HORIZONTAL PULSE TIMING <CCIR>



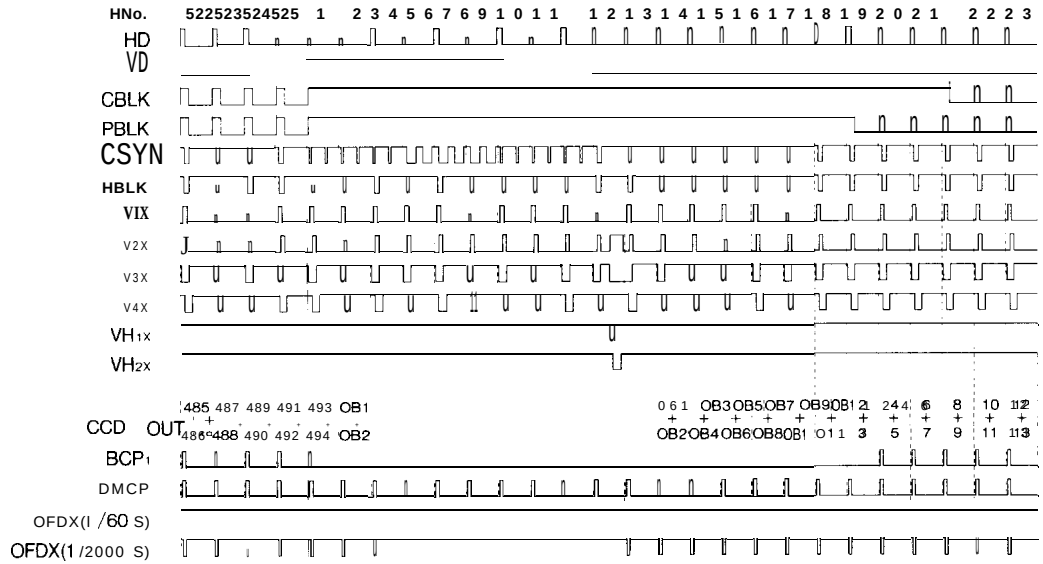
HORIZONTAL PULSE TIMING <CCIR>



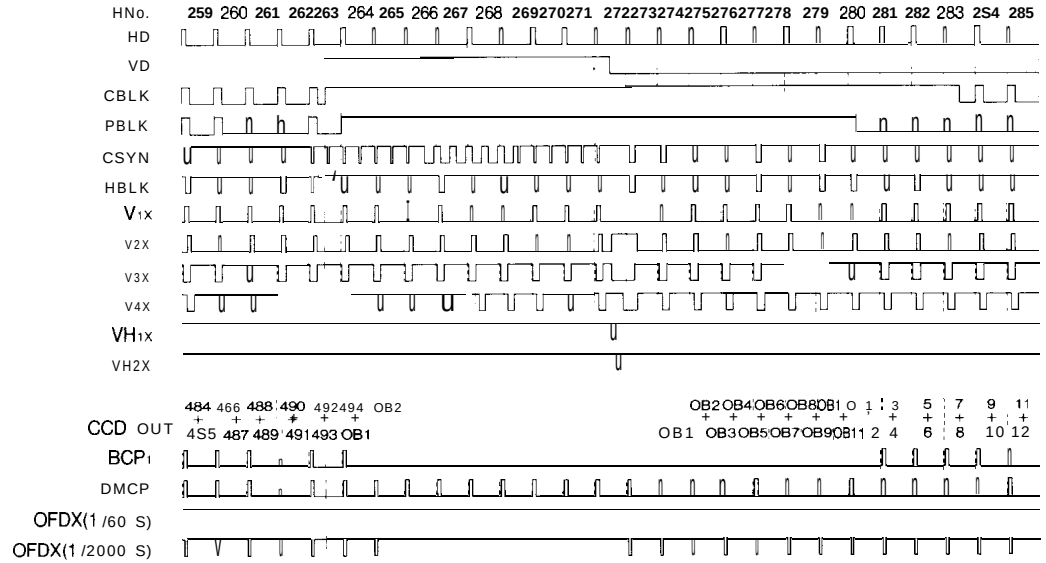


VERTICAL PULSE TIMING < EIA >

(ODD FIELD)

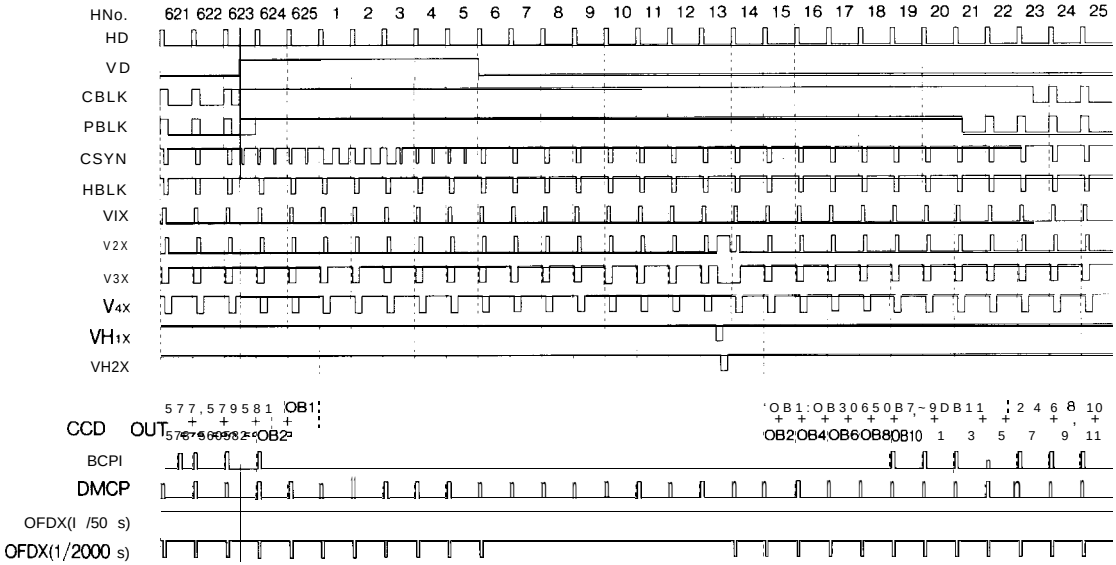


(EVEN FIELD)

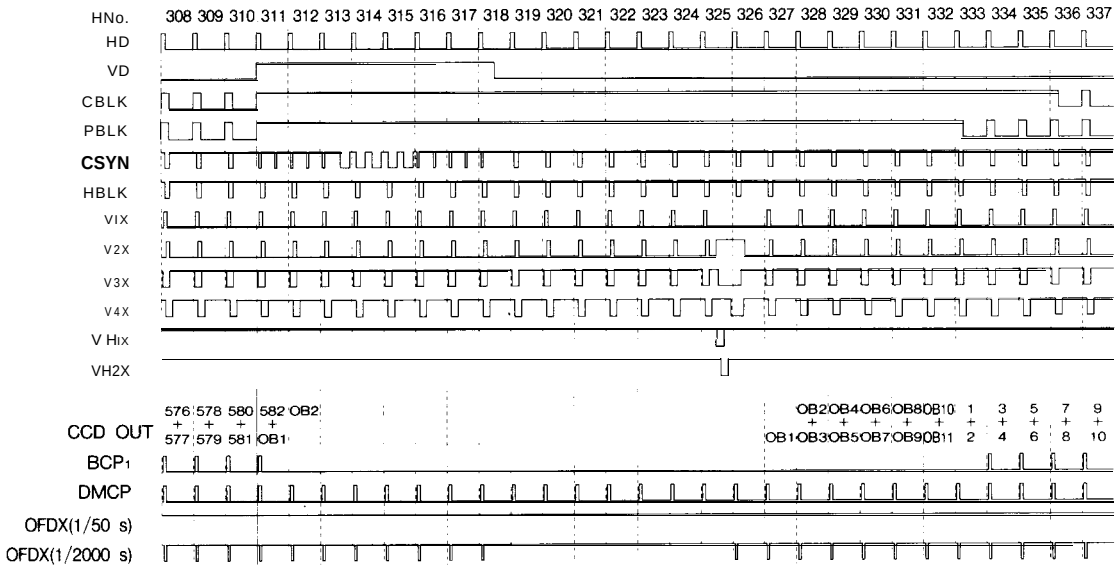


VERTICAL PULSE TIMING <CCIR>

(I at, 3rd FIELD)

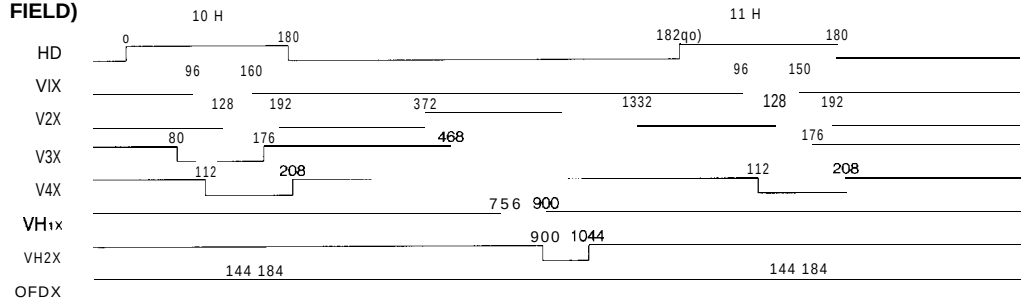


(2nd, 4th FIELD)

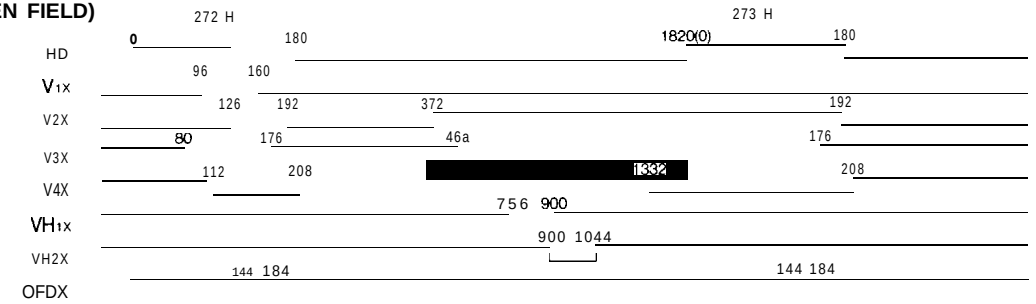


READOUT PULSE TIMING < EIA >

(ODD FIELD)

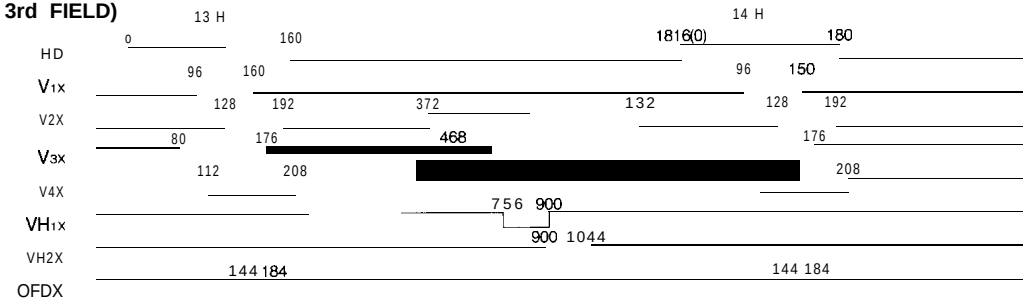


(EVEN FIELD)

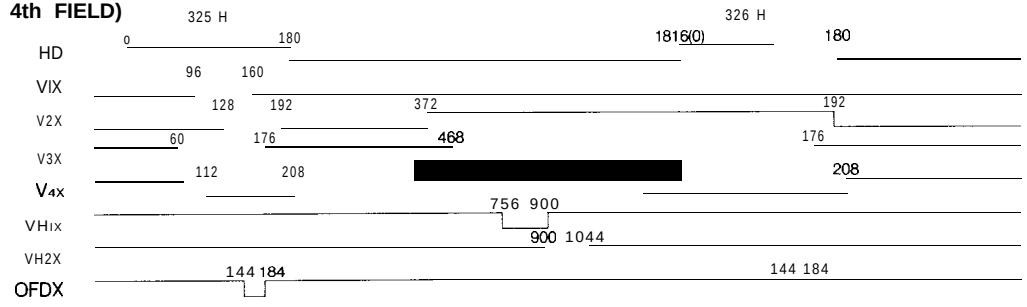


READOUT PULSE TIMING < EIA >

(I St, 3rd FIELD)

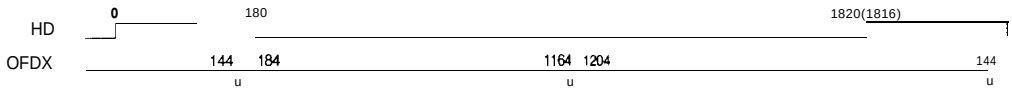


(2nd, 4th FIELD)

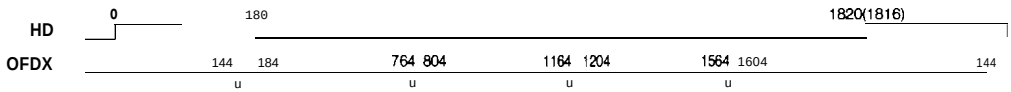


"OFDX" PULSE TIMING

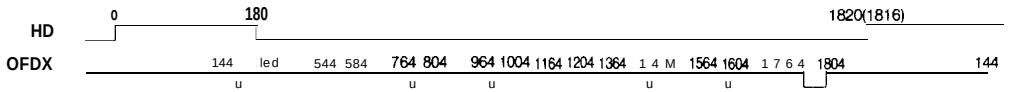
EIA : 3 to 5 H, 265 to 267 H
CCIR : **6t08 H, 318t0320 H**



EIA :6t08H,266t0270H
CCIR : **9 to 11 H, 321 to 323 H**



EIA : 9 H, 271 H
CCIR : 12 H, 324 H



EIA : 10 H, 271 H
CCIR : **13 H. 325 H**